DATA SHEET

BSH299
P-channel enhancement mode MOS transistor

Objective specification
File under Discrete Semiconductors, SC13b

1998 Feb 18

Philips Semiconductors

PHILIPS

P-channel enhancement mode MOS transistor BSH299

FEATURES

- Low threshold voltage
- High-speed switching
- No secondary breakdown
- Direct interface to C-MOS, TTL, etc.

APPLICATIONS

- Power management
- Battery powered applications e.g. cellular phones
- General purpose switch.

DESCRIPTION

P-channel enhancement mode MOS transistor in a SOT363 SMD package.

CAUTION
The device is supplied in an antistatic package. The gate-source input must be protected against static discharge during transport or handling.

PINNING - SOT363

PIN	SYMBOL	DESCRIPTION
1	d	drain
2	d	drain
3	g	gate
4	s	source
5	d	drain
6	d	drain

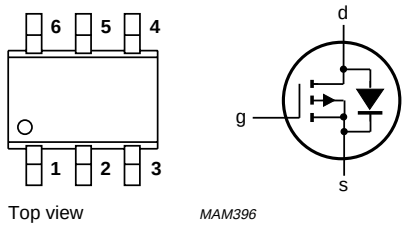


Fig.1 Simplified outline and symbol.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage (DC)		–	–50	V
V_{GSO}	gate-source voltage (DC)	open drain	–	±20	V
V_{GSth}	gate-source threshold voltage	I_D = –1 mA; V_{DS} = V_{GS}	–0.8	–2	V
I_D	drain current (DC)	T_s = 80 °C	–	–0.2	A
R_{DSon}	drain-source on-state resistance	I_D = –0.13 A; V_{GS} = –10 V	–	10	Ω
P_{tot}	total power dissipation	T_s = 80 °C	–	0.7	W

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage (DC)		–	–50	V
V_{GSO}	gate-source voltage (DC)	open drain	–	±20	V
I_D	drain current (DC)	T_s = 80 °C; note 1	–	–0.2	A
I_{DM}	peak drain current	note 2	–	–0.8	A
P_{tot}	total power dissipation	T_s = 80 °C; see Fig.2	–	0.7	W
		T_{amb} = 25 °C; note 3; see Fig.2	–	0.98	W
		T_{amb} = 25 °C; note 4; see Fig.2	–	0.66	W
T_{stg}	storage temperature		–55	+150	°C
T_j	operating junction temperature		–55	150	°C

Notes

1. T_s is the temperature at the soldering point of the drain lead.
2. Pulse width and duty cycle limited by maximum junction temperature.
3. Device mounted on a printed-circuit board with an $R_{th\ a\text{-}tp}$ (ambient to tie-point) of 27.5 K/W.
4. Device mounted on a printed-circuit board with an $R_{th\ a\text{-}tp}$ (ambient to tie-point) of 90 K/W.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}s}$	thermal resistance from junction to soldering point; see Fig.4	100	K/W

CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0; I_D = –10 μA	–50	–	–	V
V_{GSth}	gate-source threshold voltage	V_{GS} = V_{DS}; I_D = –1 mA	–0.8	–	–2	V
I_{DSS}	drain-source leakage current	V_{GS} = 0; V_{DS} = –40 V	–	–	–100	nA
		V_{GS} = 0; V_{DS} = –50 V	–	–	–10	μA
		V_{GS} = 0; V_{DS} = –50 V; T_j = 125 °C	–	–	–60	μA
I_{GSS}	gate leakage current	V_{GS} = ±20 V; V_{DS} = 0	–	–	±10	nA
R_{DSon}	drain-source on-state resistance	V_{GS} = –10 V; I_D = –0.13 A; see Fig.10	–	–	10	Ω
$\|y_{fs}\|$	forward transfer admittance	V_{DS} = –25 V; I_D = –0.13 A	50	–	–	mS
C_{iss}	input capacitance	V_{GS} = 0; V_{DS} = –25 V; f = 1 MHz; see Fig.7	–	25	45	pF
C_{oss}	output capacitance		–	15	25	pF
C_{rss}	reverse transfer capacitance		–	3.5	12	pF
Switching times (see Figs 5 and 6)						
t_{on}	turn-on switching time	V_{GS} = 0 to –10 V; V_{DD} = –40 V; I_D = –0.2 A	–	3	–	ns
t_{off}	turn-off switching time	V_{GS} = –10 to 0 V; V_{DD} = –40 V; I_D = –0.2 A	–	7	–	ns

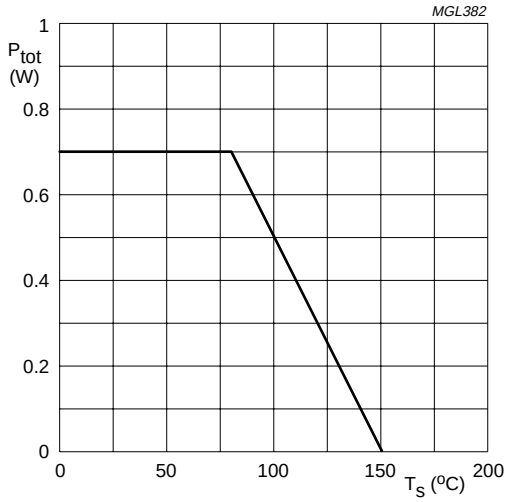


Fig.2 Power derating curve.

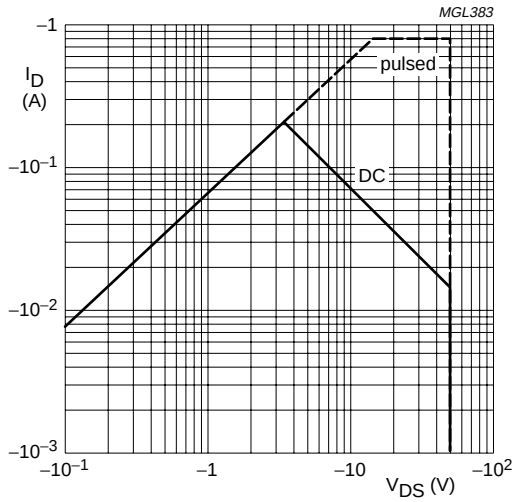


Fig.3 SOAR.

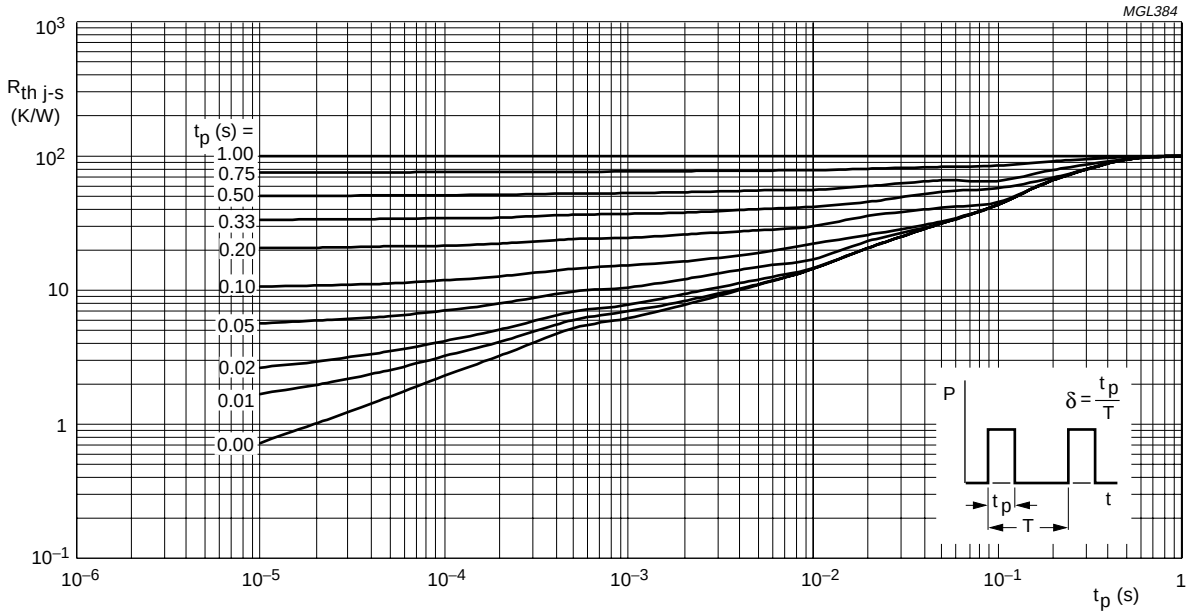


Fig.4 Transient thermal resistance from junction to soldering point as a function of pulse time; typical values.

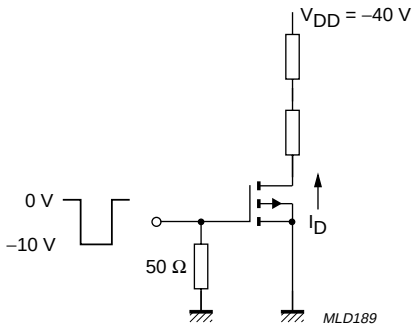


Fig.5 Switching time test circuit.

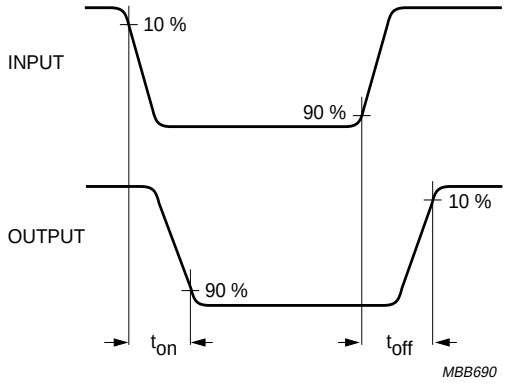
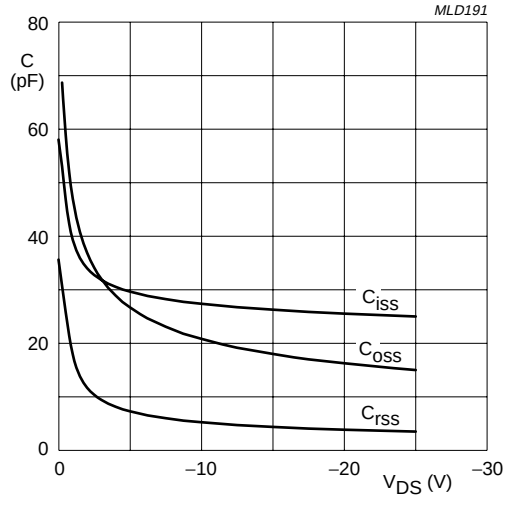
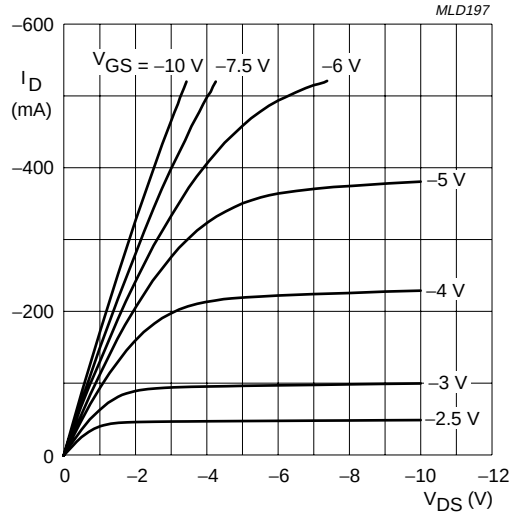


Fig.6 Input and output waveforms.



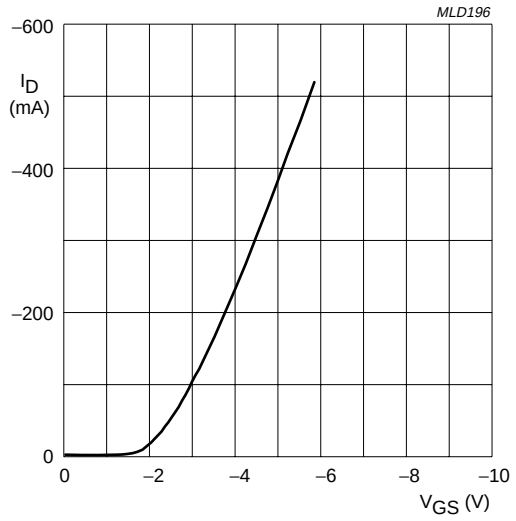
V_{GS} = 0; T_j = 25 °C; f = 1 MHz.

Fig.7 Capacitance as a function of drain-source voltage; typical values.



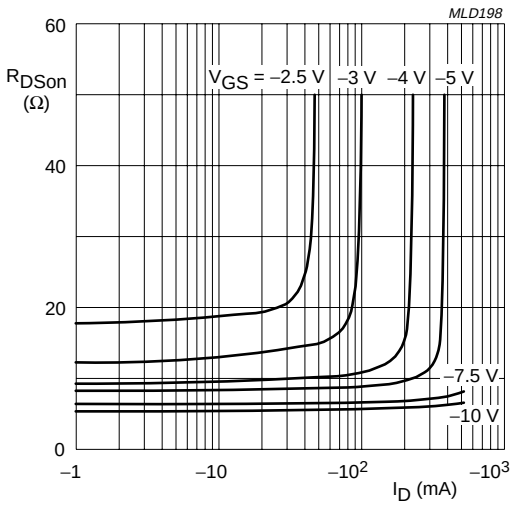
T_j = 25 °C.

Fig.8 Output characteristics; typical values.



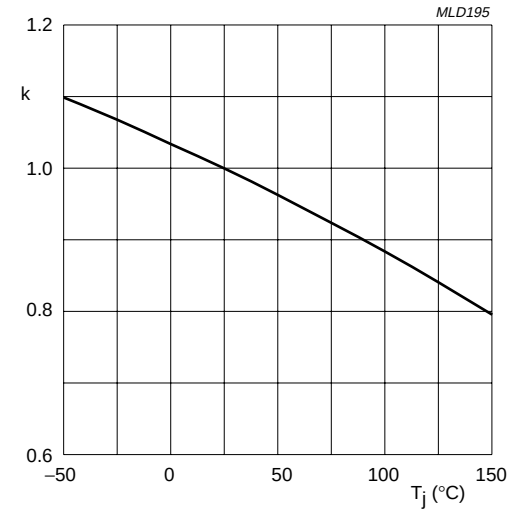
V_{DS} = −10 V; T_j = 25 °C.

Fig.9 Transfer characteristics; typical values.



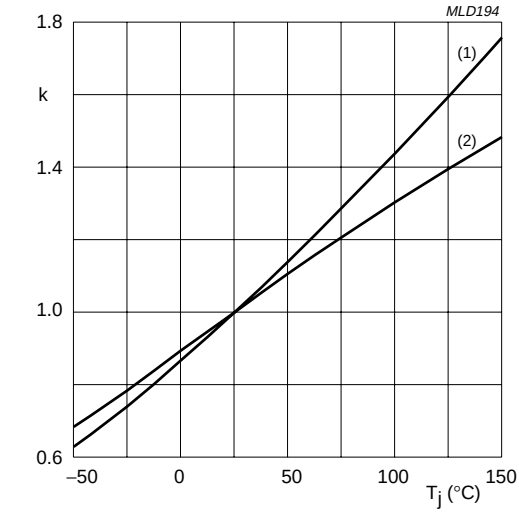
T_j = 25 °C; t_p = 300 μs; δ = 0.

Fig.10 Drain-source on-state resistance as a function of drain current; typical values.



k = (V_{GSth} at T_j)/(V_{GSth} at 25 °C).
I_D = −1 mA; V_{DS} = V_{GS}.

Fig.11 Temperature coefficient of gate-source threshold voltage as a function of junction temperature; typical values.

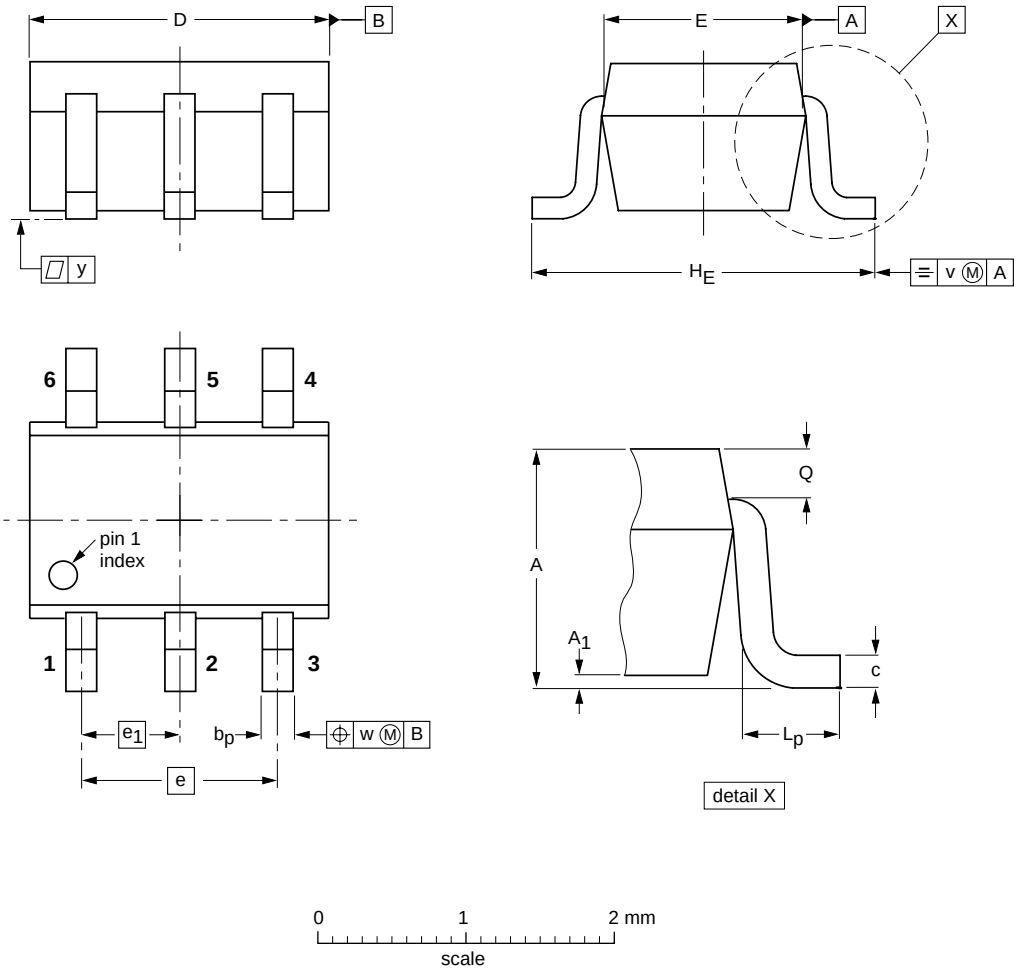


k = (R_{DSon} at T_j)/(R_{DSon} at 25 °C).
(1) I_D = −130 mA; V_{GS} = −10 V.
(2) I_D = −20 mA; V_{GS} = −2.4 V.

Fig.12 Temperature coefficient of drain-source on-resistance as a function of junction temperature; typical values.

PACKAGE OUTLINE

Plastic surface mounted package; 6 leads **SOT363**



DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1 max	b_p	c	D	E	e	e_1	H_E	L_p	Q	v	w	y
mm	1.1 0.8	0.1	0.30 0.20	0.25 0.10	2.2 1.8	1.35 1.15	1.3	0.65	2.2 2.0	0.45 0.15	0.25 0.15	0.2	0.2	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT363			SC-88			97-02-28

DEFINITIONS

Data Sheet Status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

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Printed in The Netherlands 135108/00/01/pp12 Date of release: 1998 Feb 18 Document order number: 9397 750 03223

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